Serial No.: 10/734,994

Filed: December 12, 2003

Page : 3 of 11

## Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

## Listing of Claims:

1. (Original) A microlithography method including:

interferometrically measuring information about a position of a microlithography stage with respect to each of multiple metrology axes during a photolithographic exposure cycle;

analyzing the position information to determine correction factors indicative of a local slope on a side of the stage used to reflect an interferometric measurement beam and optical gradients caused by environmental effects produced by the photolithographic exposure cycle; and

applying the correction factors to subsequent interferometric measurements of the stage.

- 2. (Original) The method of claim 1, wherein the stage carries a wafer exposed to illumination light during the photolithographic exposure cycle.
- 3. (Original) The method of claim 1, wherein the stage carries a reticle through which illumination light passes to expose a wafer during the photolithographic exposure cycle.
- 4. (Original) The method of claim 1, wherein the information is measured when exposing a first region of a wafer during the photolithography exposure cycle, and wherein the correction factors are applied to subsequent interferometric measurements of

Serial No.: 10/734,994

Filed: December 12, 2003

Page : 4 of 11

the stage when exposing subsequent regions or layers of the wafer during the photolithography exposure cycle.

5. (Original) The method of claim 1, wherein the information is measured when exposing a first region of a wafer during the photolithography exposure cycle, and wherein the correction factors are applied to subsequent interferometric measurements of the stage when exposing a region of another wafer during its photolithography exposure cycle.

- 6. (Original) The method of claim 1, wherein the correction factors are determined based on averaging information for multiple scans of the stage along at least a first direction.
- 7. (Original) The method of claim 1, wherein the position information is measured using at least one high stability plane mirror interferometer.
- 8. (Original) The method of claim 1, wherein the position information is measured using at least one single beam interferometer.
- 9. (Original) The method of claim 8, wherein the single beam interferometer is a dynamic single beam interferometer.
- 10. (Original) The method of claim 8, wherein the single beam interferometer is a passive single beam interferometer.
- 11. (Original) The method of claim 1, wherein the correction factors are indicative of the local slope on at least two sides of the stage used to reflect an interferometric measurement beam.

Serial No.: 10/734,994

Filed: December 12, 2003

Page : 5 of 11

12. (Original) The method of claim 1, wherein the correction factors are indicative of the local slope of the side of the stage along an in-plane direction.

- 13. (Original) The method of claim 1, wherein the multiple metrology axes provide redundant information about the stage position in the absence of the local slope and optical gradient variations.
- 14. (Original) A method comprising fabricating integrated circuits using the lithography method of claim 1.
  - 15. (New) A microlithography method including:

interferometrically measuring information about a position of a microlithography stage with respect to each of multiple metrology axes during a photolithographic exposure cycle using a single-wavelength interferometer;

analyzing the position information to determine correction factors indicative of a local slope on a side of the stage used to reflect an interferometric measurement beam and optical gradients caused by environmental effects produced by the photolithographic exposure cycle; and

applying the correction factors to subsequent interferometric measurements of the stage.

- 16. (New) The method of claim 15, wherein the stage carries a wafer exposed to illumination light during the photolithographic exposure cycle.
- 17. (New) The method of claim 15, wherein the stage carries a reticle through which illumination light passes to expose a wafer during the photolithographic exposure cycle.

Serial No.: 10/734,994

Filed: December 12, 2003

Page : 6 of 11

18. (New) The method of claim 15, wherein the information is measured when exposing a first region of a wafer during the photolithography exposure cycle, and wherein the correction factors are applied to subsequent interferometric measurements of the stage when exposing subsequent regions or layers of the wafer during the photolithography exposure cycle.

- 19. (New) The method of claim 15, wherein the information is measured when exposing a first region of a wafer during the photolithography exposure cycle, and wherein the correction factors are applied to subsequent interferometric measurements of the stage when exposing a region of another wafer during its photolithography exposure cycle.
- 20. (New) The method of claim 15, wherein the correction factors are determined based on averaging information for multiple scans of the stage along at least a first direction.
- 21. (New) The method of claim 15, wherein the position information is measured using at least one high stability plane mirror interferometer.
- 22. (New) The method of claim 15, wherein the position information is measured using at least one single beam interferometer.
- 23. (New) The method of claim 15, wherein the correction factors are indicative of the local slope on at least two sides of the stage used to reflect an interferometric measurement beam.

Serial No.: 10/734,994

Filed: December 12, 2003

Page : 7 of 11

24. (New) The method of claim 15, wherein the correction factors are indicative of the local slope of the side of the stage along an in-plane direction.

- 25. (New) The method of claim 15, wherein the multiple metrology axes provide redundant information about the stage position in the absence of the local slope and optical gradient variations.
- 26. (New) A method comprising fabricating integrated circuits using the lithography method of claim 15.